CLAIMS

What is claimed is:

1. A method, comprising:

setting a memory used by a bus master device as non-cacheable, the memory and the bus master device being in a computer system;

not setting a bus master status bit (BM_STS) for any bus master memory operation by the bus master device with the memory; and

placing the processor in the computer system into a low power state

2. The method of claim 1, wherein the low power state is a deep sleep state.

3. The method of claim 1, wherein the low power state is a C3 state.

4. The method of claim 1, wherein the memory is coupled to a memory subsystem which does not generate snoop cycles to the processor during any bus master accesses performed by the bus master device.

5. The method of claim 4, wherein the bus master device is allowed to generate bus master read and write operations when the ARB_DIS bit is set.

6. A computer readable medium having stored thereon sequences of instructions which are executable by a system, and which, when executed by the system, cause the system to perform a method, comprising:

setting a memory used by a bus master device as non-cacheable, the memory and the bus master device are in a computer system;

not setting a bus master status bit (BM_STS) for any bus master memory operation by the bus master device with the memory; and

placing the processor in the computer system into a low power state

7. The computer readable medium of claim 6, wherein the low power state is a deep sleep state.

8. The computer readable medium of claim 6, wherein the low power state is a C3 state.

9. The computer readable medium of claim 6, wherein the memory is coupled to a memory subsystem which does not generate snoop cycles to the processor during any bus master accesses performed by the bus master device.

10. The computer readable medium of claim 9, wherein the bus master device is allowed to generate bus master read and write operations when the ARB_DIS bit is set.

11. A system, comprising:

a memory set as non-cacheable;

a bus master device coupled to the memory; and

a processor coupled to the memory and the bus master device, wherein the processor is placed into a low power state while the bus master device performs memory operations with the non-cacheable memory and while a bus master status (BM_STS) bit is not set for these bus operations.

12. The system of claim 11, wherein the low power state is a deep sleep state.

13. The system of claim 11, wherein the low power state is a C3 state.

14. The system of claim 11, further comprising a memory subsystem coupled to the memory, wherein the memory subsystem does not generate snoop cycles to the processor during any memory operations performed by the bus master device

15. The system of claim 14, wherein the bus master device is allowed to generate bus master read and write operations when an arbiter disable (ARB_DIS) bit is set.

16. A method, comprising:

setting a memory used by a bus master device as write through-cacheable, the memory and the bus master device are in a computer system;

not setting the bus master status (BM_STS) bit while the bus master device performs memory read operations with the memory; and

placing the processor in the computer system into a low power state

17. The method of claim 16, further comprising setting the BM_STS bit while the bus master device performs memory write operations with the memory.

18. The method of claim 17, wherein the processor is not placed in the low power state while the bus master device performs memory write operations with the memory.

19. The method of claim 17, wherein the low power state is a C3 state.

20. The method of claim 16, wherein the memory is coupled to a memory subsystem which does not generate snoop cycles to the processor during any bus master read operations performed by the bus master device

21. The method of claim 20, wherein the bus master device is allowed to generate bus master read operations when the ARB_DIS bit is set

22. A computer readable medium having stored thereon sequences of instructions which are executable by a system, and which, when executed by the system, cause the system to perform a method, comprising:

setting a memory used by a bus master device as write-through-cacheable, the memory and the bus master device are in a computer system;

not setting a bus master status (BM_STS) bit while the bus master device performs memory read operations with the memory; and

placing a processor in the computer system into a low power state.

23. The computer readable medium of claim 22, further comprising setting the BM_STS bit while bus master device performs memory write operations with the memory.

24. The computer readable medium of claim 22, wherein the processor is not placed in the low power state while bus master device performs memory write operations with the memory.

25. The computer readable medium of claim 22, wherein the low power state is a C3 state.

26. The computer readable medium of claim 22, wherein the memory is coupled to a memory subsystem which does not generate snoop cycles to the processor during any bus master read accesses performed by the bus master device

27. The computer readable medium of claim 26, wherein the bus master device is allowed to generate bus master read operations when the ARB_DIS bit is set

28. A system, comprising:

a memory set as write-through cacheable;

a bus master device coupled to the memory; and

a processor coupled to the memory and the bus master device, wherein

the bus master is allowed to perform memory read operations while the processor is in a low power state without setting the bus master status (BM_STS) bit.

29. The system of claim 28, wherein the processor is not placed into the low power state while the bus master device performs memory write operations with the memory.

30. The system of claim 28, wherein the BM_STS bit is set while the bus master device performs the memory write operations with the memory.

31. The system of claim 28, wherein the low power state is a C3 state.

32. The system of claim 28, further comprising a memory subsystem coupled to the memory, wherein the memory subsystem does not generate snoop cycles to the processor during any bus master read operations performed by the bus master device.

33. The system of claim 32, wherein the bus master device is allowed to generate bus master read operations when the ARB_DIS bit is set.